What Is Claimed:

1. An improved trench MOS-gated device comprising:

a substrate comprising doped monocrystalline semiconductor material;

a doped upper layer disposed on said substrate, said upper layer having an upper surface and comprising at said upper surface a plurality of heavily doped body regions having a first polarity, said body regions overlying a drain region in said upper layer, said upper layer further comprising at said upper surface a plurality of heavily doped source regions having a second polarity and extending from said upper surface to a selected depth in said upper layer; and

a gate trench separating one of said source regions from a second source region, said trench extending from said upper surface of said upper layer to said drain region, said trench having a floor and sidewalls comprising a layer of dielectric material, said trench being filled with a conductive gate material to a selected level substantially below the upper surface of the upper layer and with an isolation layer of dielectric material overlying said gate material, said overlying layer of dielectric material in said trench having an upper surface that is substantially coplanar with said upper surface of said upper layer.

2. The device of claim 1 wherein said substrate comprises monocrystalline silicon.

3. The device of claim 1 wherein said upper layer comprises an epitaxial layer.

4. The device of claim 1 wherein said upper layer comprises a heavily doped portion of said substrate.

5. The device of claim 1 wherein said upper layer further comprises a well region having said first polarity, said well region underlying said body and source regions and overlying said drain region.

6. The device of claim 1 wherein one of said source regions is disposed between and adjacent to one of said source regions and a gate trench.

7. The device of claim 1 wherein one of said source regions is disposed between and adjacent to two gate trenches.

8. The device of claim 1 wherein said plurality of body regions and said plurality of source regions comprise a plurality of arrays of alternating body regions and source regions each disposed adjacent to a gate trench, and wherein one of said arrays is separated from a second of said arrays by said gate trench.

9. The device of claim 8 wherein each said array of alternating body regions and source regions have a lengthwise dimension along said gate trench, said source regions comprising a greater portion and said body regions comprising a lesser portion of said lengthwise dimension.

10. The device of claim 1 wherein the selected level of gate material in the trench is substantially coplanar with the selected depth of the source regions in the upper layer.

11. The device of claim 1 wherein said dielectric material forming said sidewalls, said floor, and said isolation layer in said gate trench comprises silicon dioxide.

12. The device of claim 1 wherein said conductive gate material within said gate trench is selected from the group consisting of a metal, a silicide, and doped polysilicon.

13. The device of claim 1 wherein said first polarization is P and said second polarization is N.

14. The device of claim 1 wherein said first polarization is N and said second polarization is P.

15. The device of claim 1 comprising a plurality of gate trenches having an open-cell stripe topology.

16. The device of claim 1 comprising a plurality of gate trenches having a closed-cell cellular topology.

17. The device of claim 16 wherein cells in said closed-cell cellular topology have a square configuration or a hexagonal configuration.

18. The device of claim 1 wherein said device is a power MOSFET.

19. The device of claim 1 wherein said device is an insulated gate bipolar transistor.

20. The device of claim 1 wherein said device is an MOS-controlled thyristor.

21. A process for forming an improved trench MOS-gated device, said process comprising:

(a) forming a doped upper layer on a semiconductor substrate, said upper layer having an upper surface and an underlying drain region;

(b) forming a well region having a first polarity in said upper layer, said well region overlying said drain region;

(c) forming a gate trench mask on said upper surface of said upper layer;

(d) forming a plurality of gate trenches extending from the upper surface of said upper layer through said well region to said drain region;

(e) forming sidewalls and floor each comprising a dielectric material in each of said gate trenches;

(f) filling each of said gate trenches to a selected level substantially below the upper surface of said upper level with a conductive gate material;

(g) removing said trench mask from the upper surface of said upper layer;

(h) forming an isolation layer of dielectric material on the upper surface of

said upper layer and within said gate trench, said isolation layer overlying said gate material and substantially filling said trench;

(i) removing said dielectric layer from the upper surface of said upper layer, said dielectric layer remaining within and substantially filling said trench having an upper surface that is substantially coplanar with the upper surface of said upper layer;

(j) forming a plurality of heavily doped source regions having a second polarity in said body regions, said source regions extending to a selected depth from the upper surface of said upper layer;

(k) forming a plurality of heavily doped body regions having a first polarity at the upper surface of said upper layer, said body regions overlying the drain region in said upper layer; and

(l) forming a metal contact to said body and source regions over the upper surface of said upper layer.

22. The process of claim 21 wherein said substrate comprises monocrystalline silicon.

23. The process of claim 21 wherein said upper layer comprises an epitaxial layer.

24. The process of claim 21 wherein said upper layer comprises a heavily doped portion of said substrate.

25. The process of claim 21 wherein one of said source regions is disposed between and adjacent to one of said source regions and a gate trench.

26. The process of claim 21 wherein one of said source regions is disposed between and adjacent to two gate trenches.

27. The process of claim 21 wherein said forming well region comprises doping said upper layer.

28. The process of claim 27 wherein said forming heavily doped body regions comprises further doping said upper layer.

29. The process of claim 21 wherein said forming heavily doped source regions comprises masked ion implanting and diffusing.

30. The process of claim 29 wherein said masked ion implanting and diffusing is to a selected depth in said doped layer that is substantially coplanar with said filling level of said gate material in said gate trench.

31. The process of claim 21 wherein the forming said source regions and said body regions comprises:

(j') implanting the entire upper surface of said substrate with a ions of said second polarity, then forming a body mask on the upper surface of said substrate, said mask comprising openings transverse to said trenches; and

(k') doping the upper surface of said substrate with a dopant of said first polarity, then removing said body mask.

32. The process of claim 21 wherein said plurality of body regions and said plurality of source regions comprise a plurality of arrays of alternating body regions and source regions each disposed adjacent to a gate trench, and wherein one of said arrays is separated from a second of said arrays by said gate trench.

33. The process of claim 32 wherein each said array of alternating body regions and source regions have a lengthwise dimension along said gate trench, said source regions comprising a greater portion and said body regions comprising a lesser portion of said lengthwise dimension.

34. The process of claim 21 wherein said dielectric material forming said sidewalls, said floor, and said isolation layer in said gate trench comprises silicon dioxide

35. The process of claim 21 wherein said conductive gate material within said gate trench is selected from the group consisting of a metal, a silicide, and doped polysilicon.

36. The process of claim 21 wherein the selected level of gate material in the trench is substantially coplanar with the selected depth of the source regions in the upper layer.

37. The process of claim 21 wherein said first polarization is P and said second polarization is N.

38. The process of claim 21 wherein said first polarization is N and said second polarization is P.

39. The process of claim 21 wherein said device is selected from the group consisting of a power MOSFET, an insulated gate bipolar transistor, an MOS-controlled thyristor, and an accumulation FET.